

Figure 2. Data Encapsulation Through the Network Stack (Prior Art)

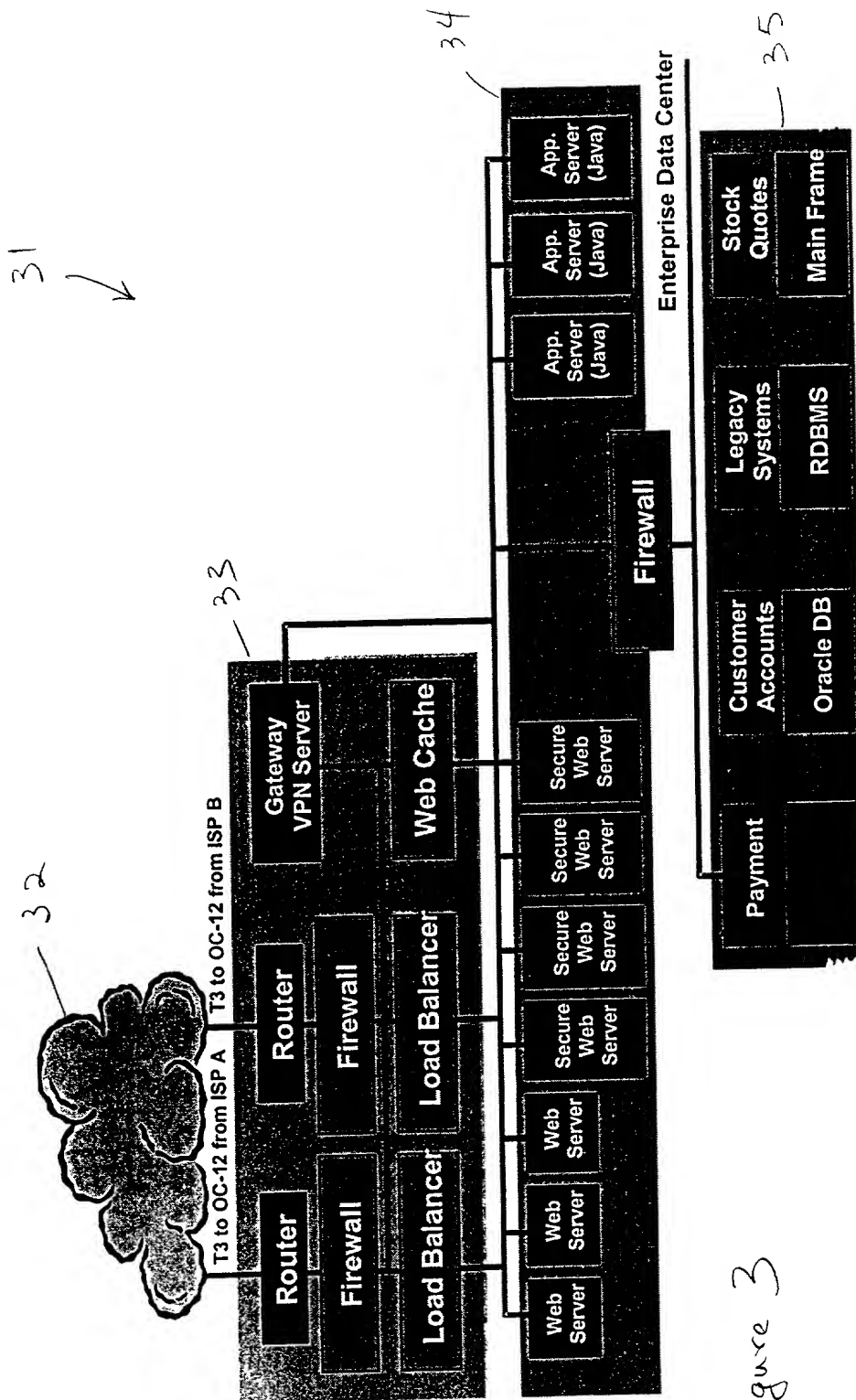


Figure 3

Fig. 4
(Prior Art)

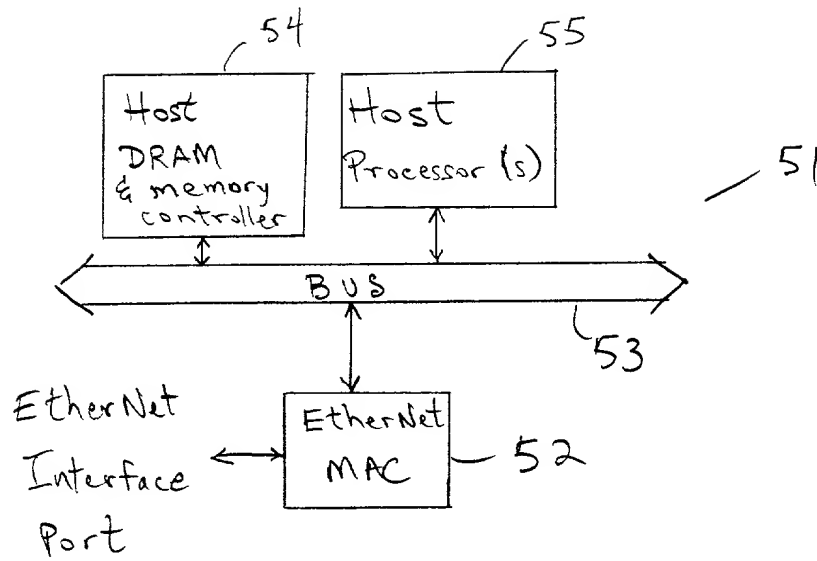
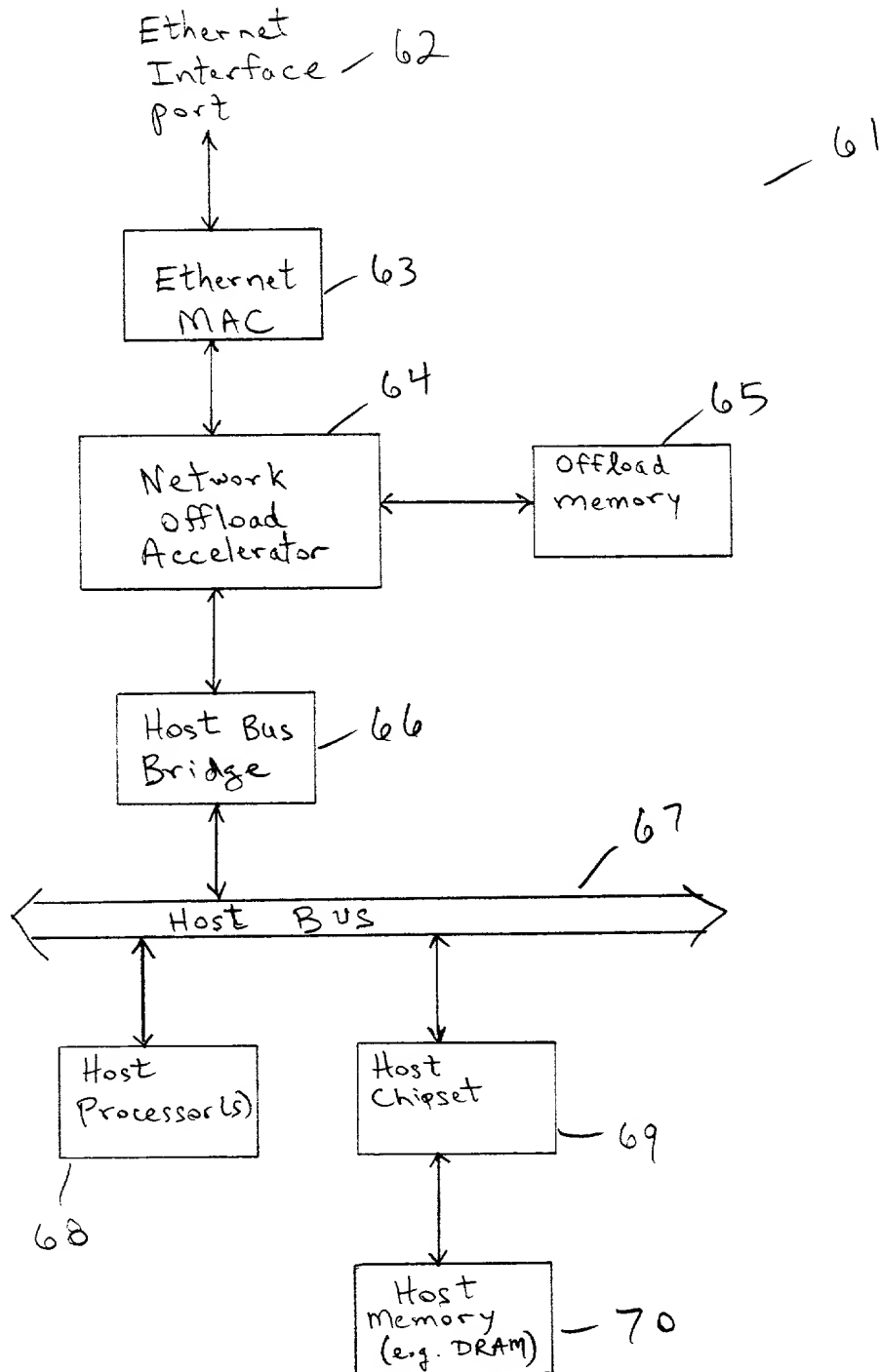


Figure 5 (prior art)



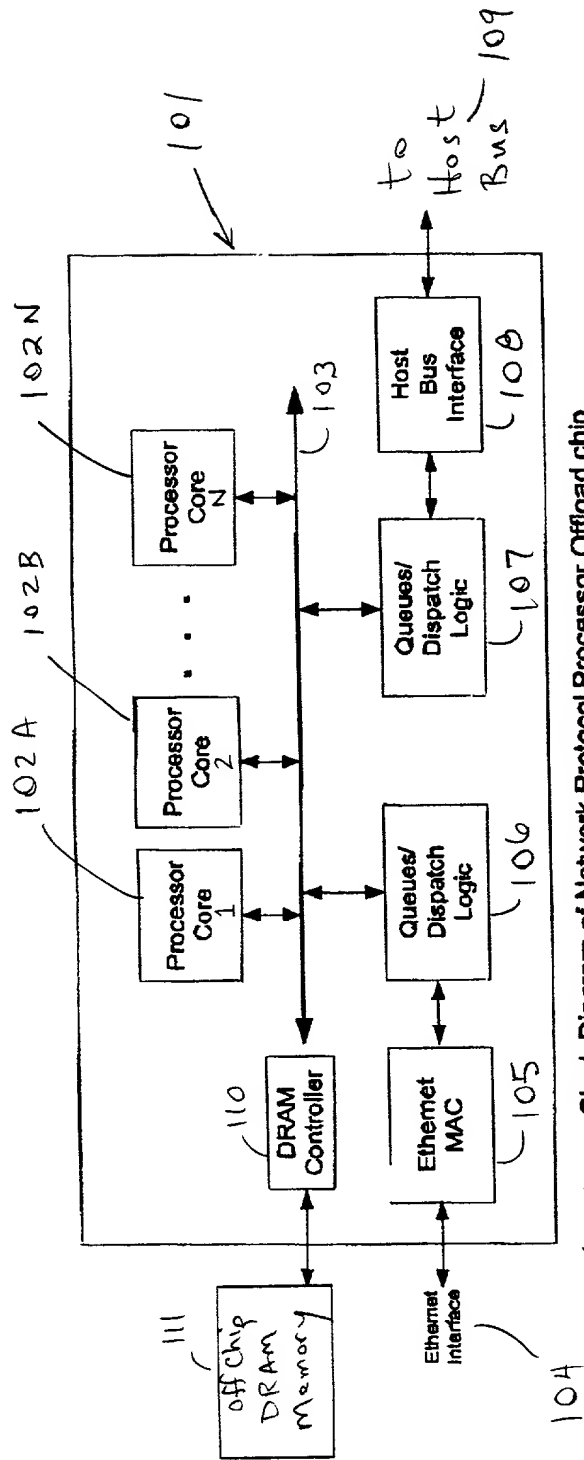
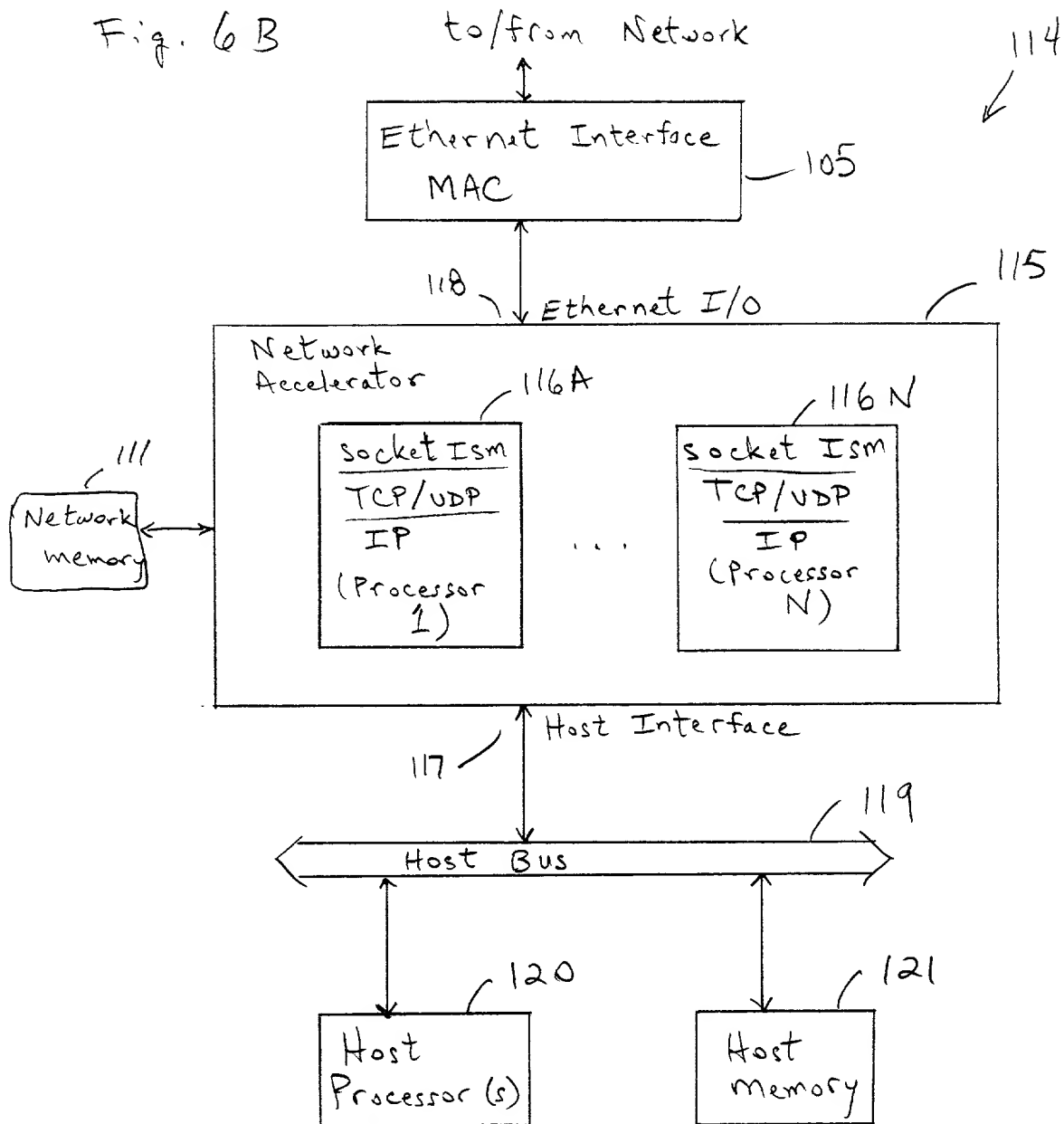


Fig. 6A Block Diagram of Network Protocol Processor Offload chip

Fig. 6B



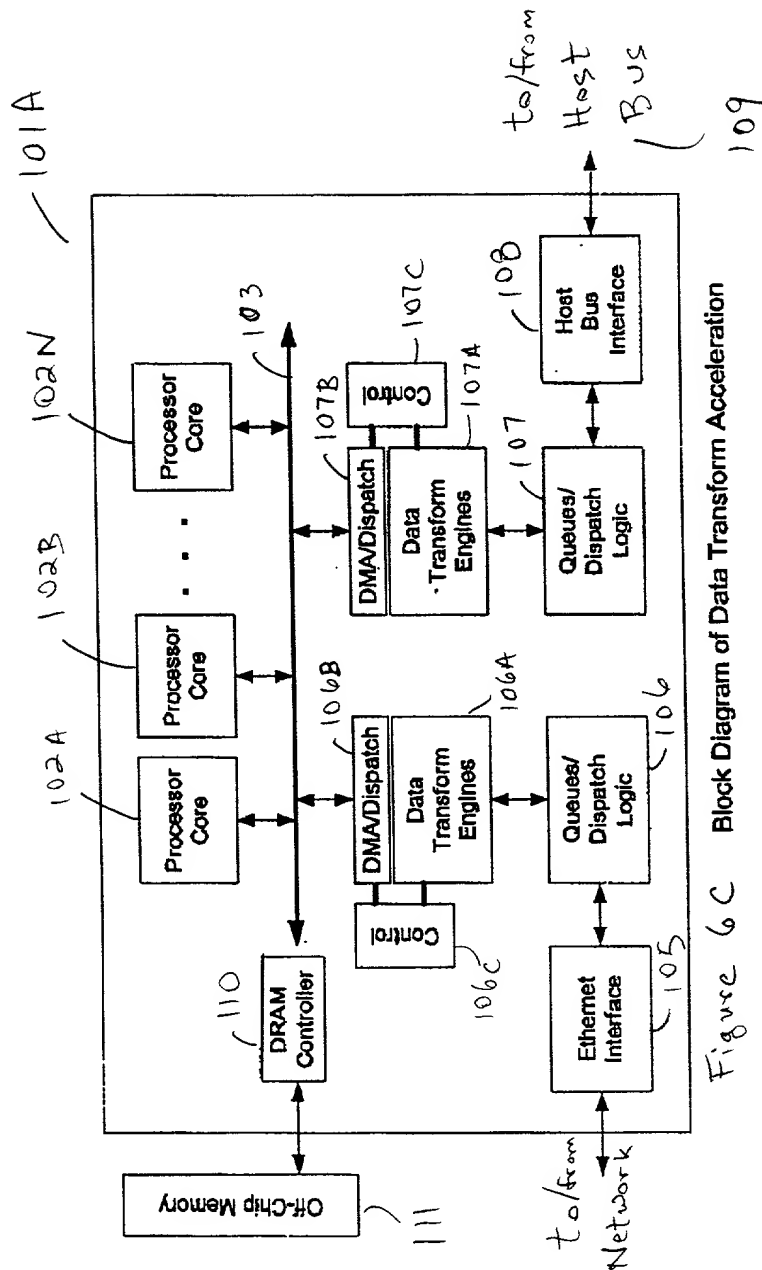


Figure 6C Block Diagram of Data Transform Acceleration

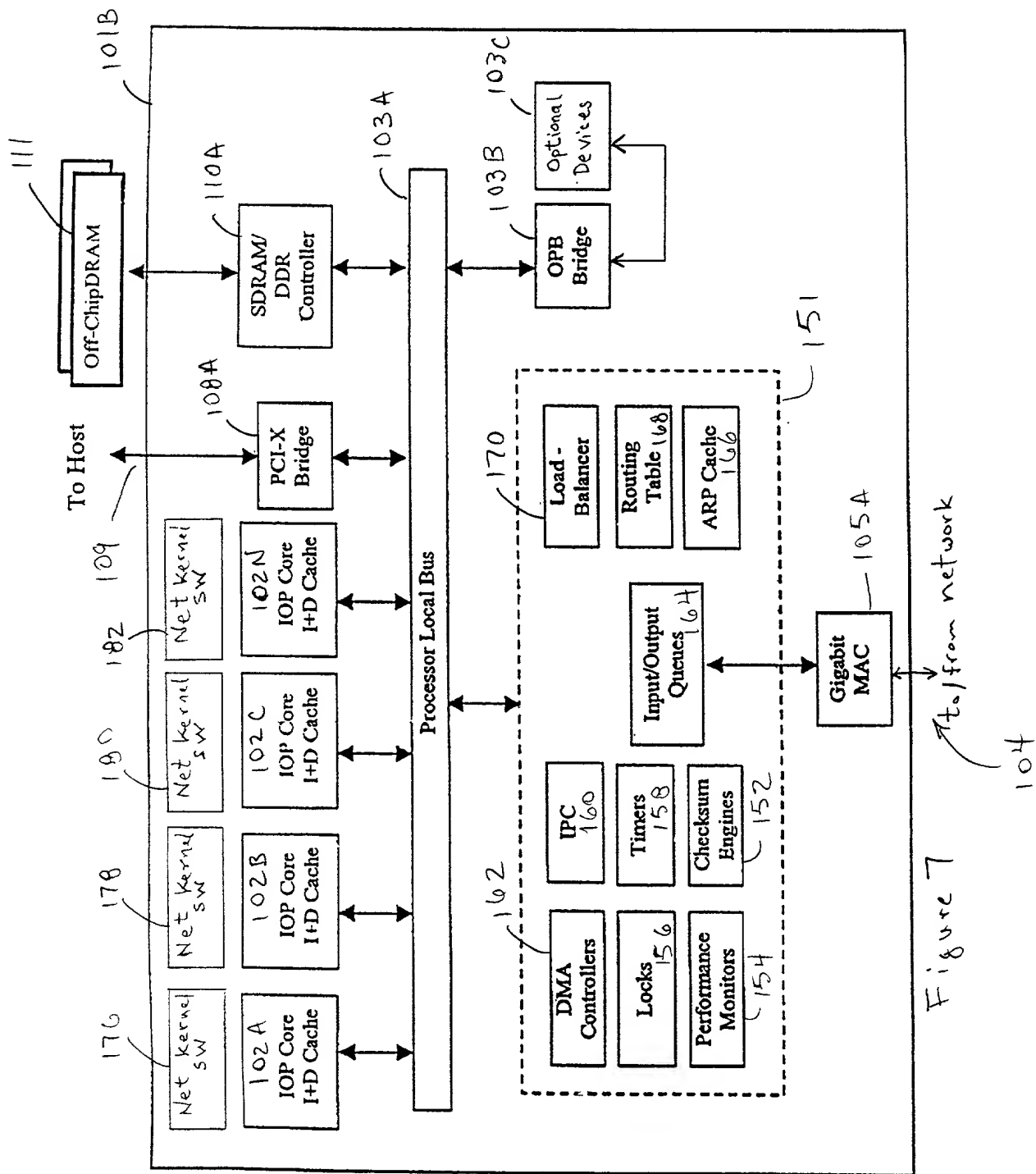


Figure 7

Fig. 8A

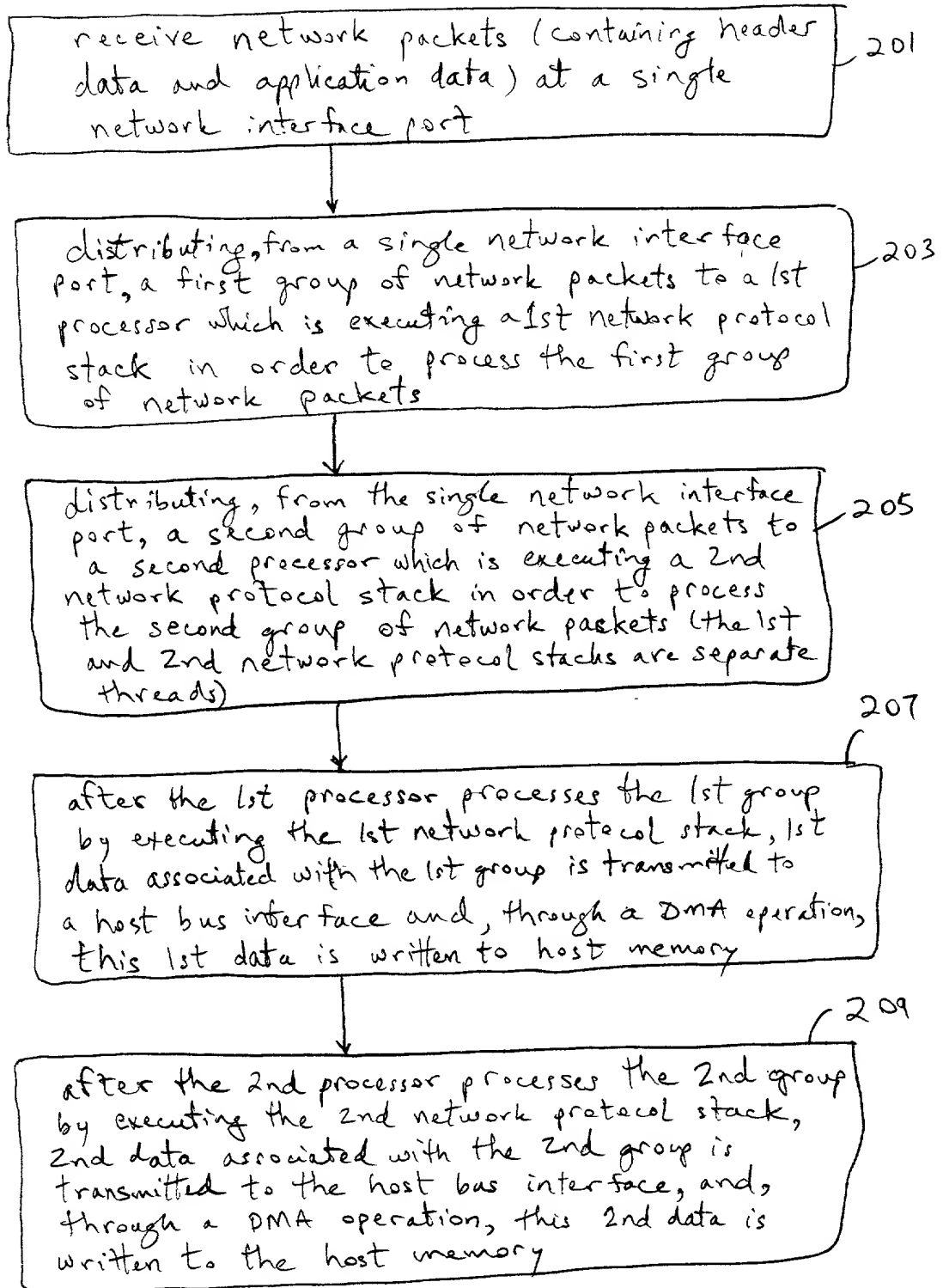


Fig. 8B

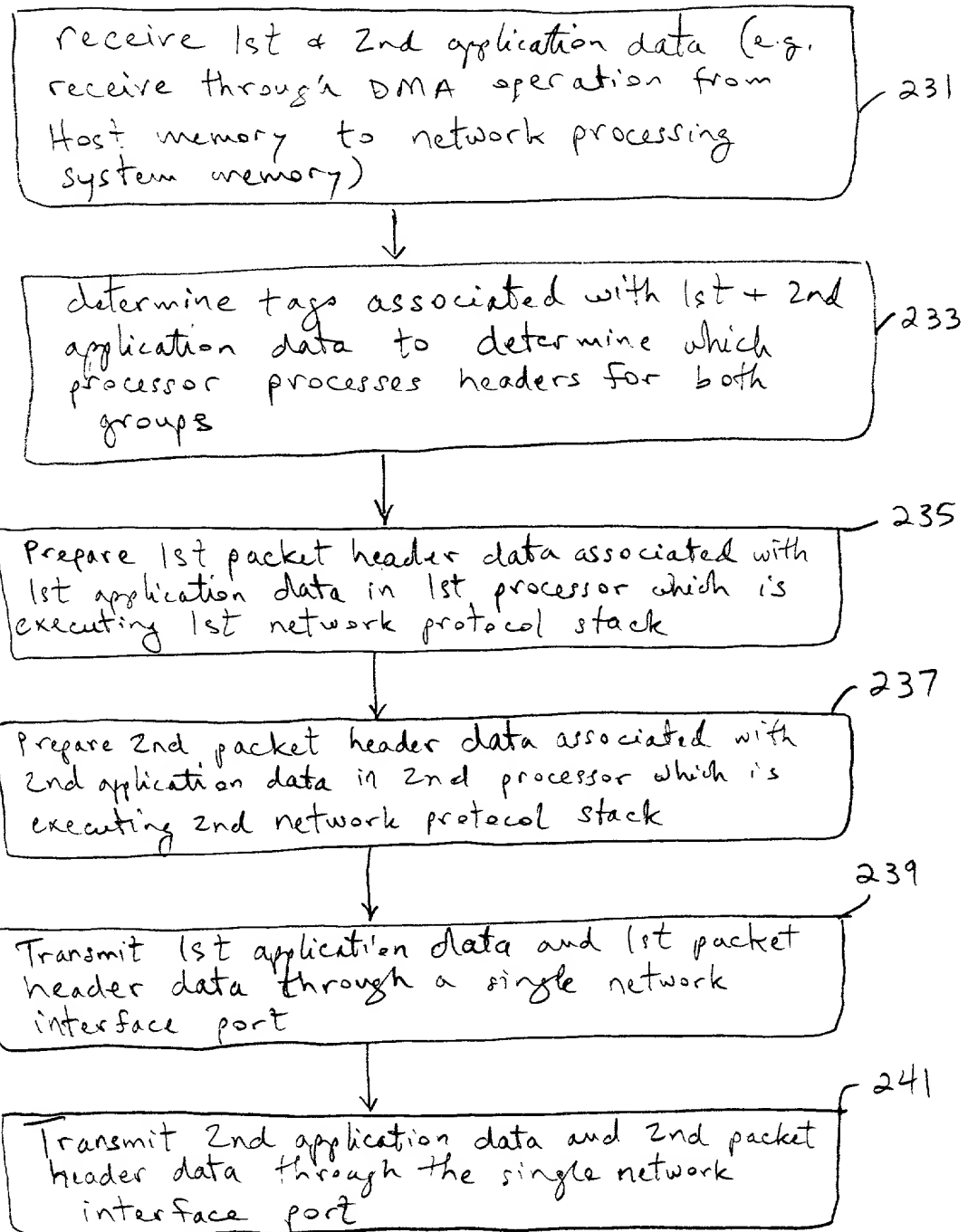


Fig. 8C

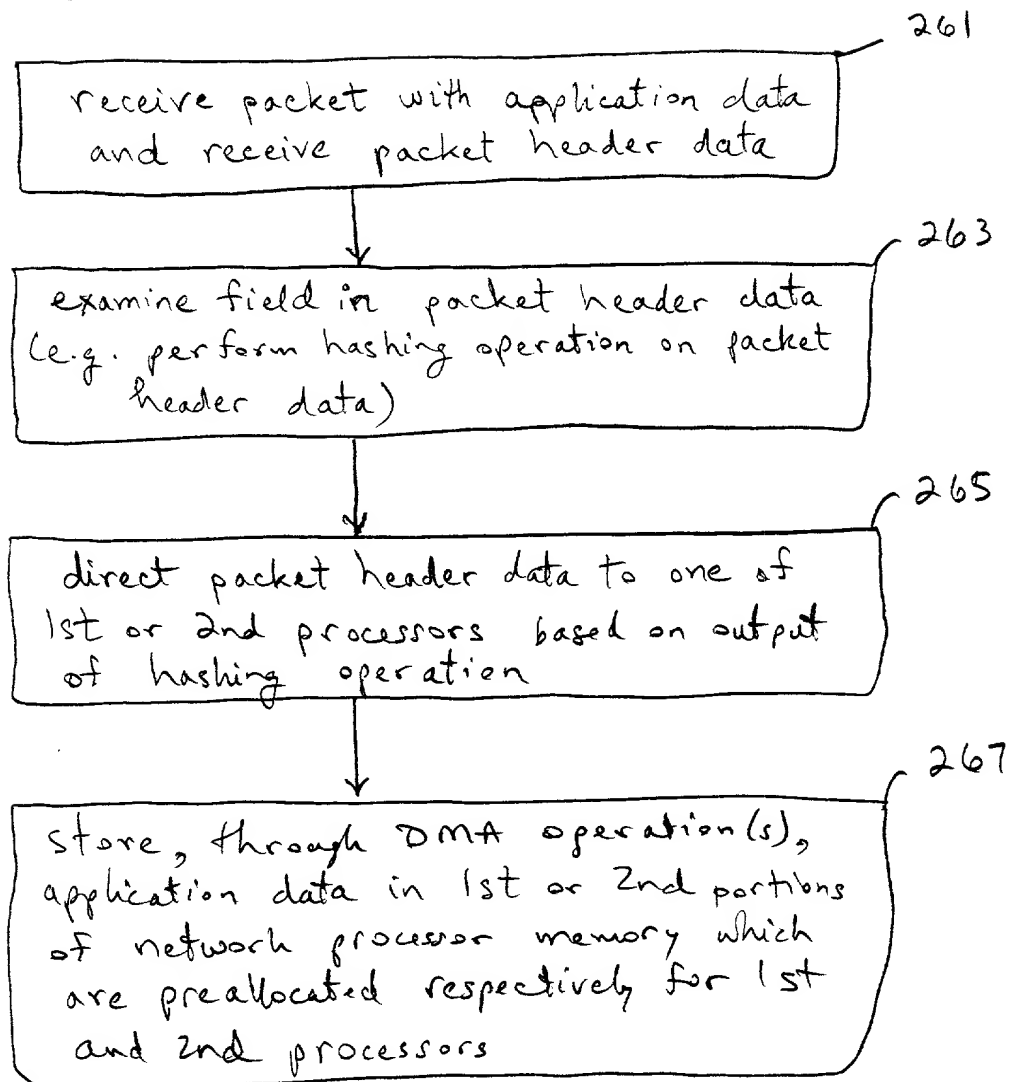
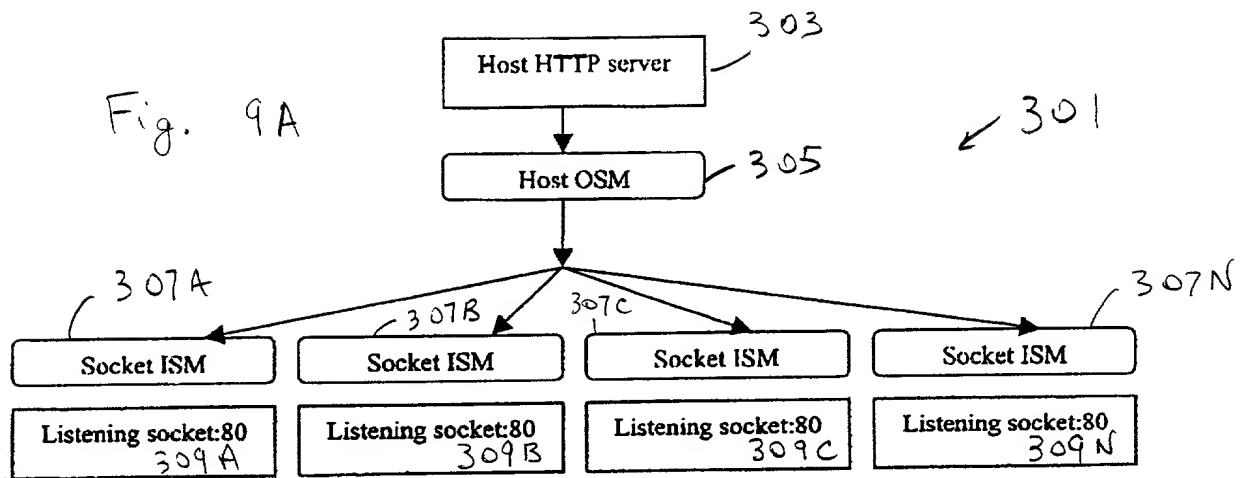
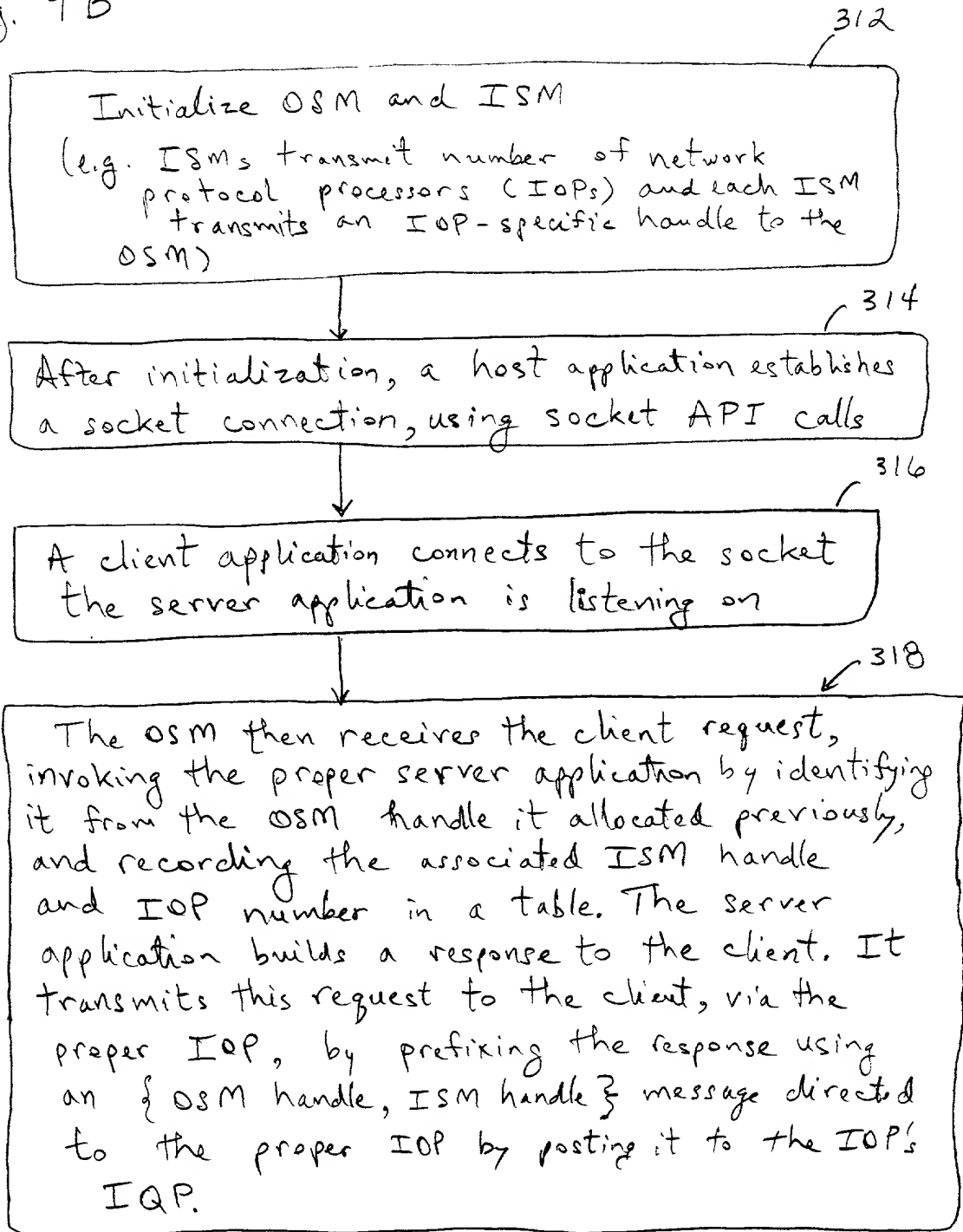


Fig. 9A



Replication of listening sockets

Fig. 9B



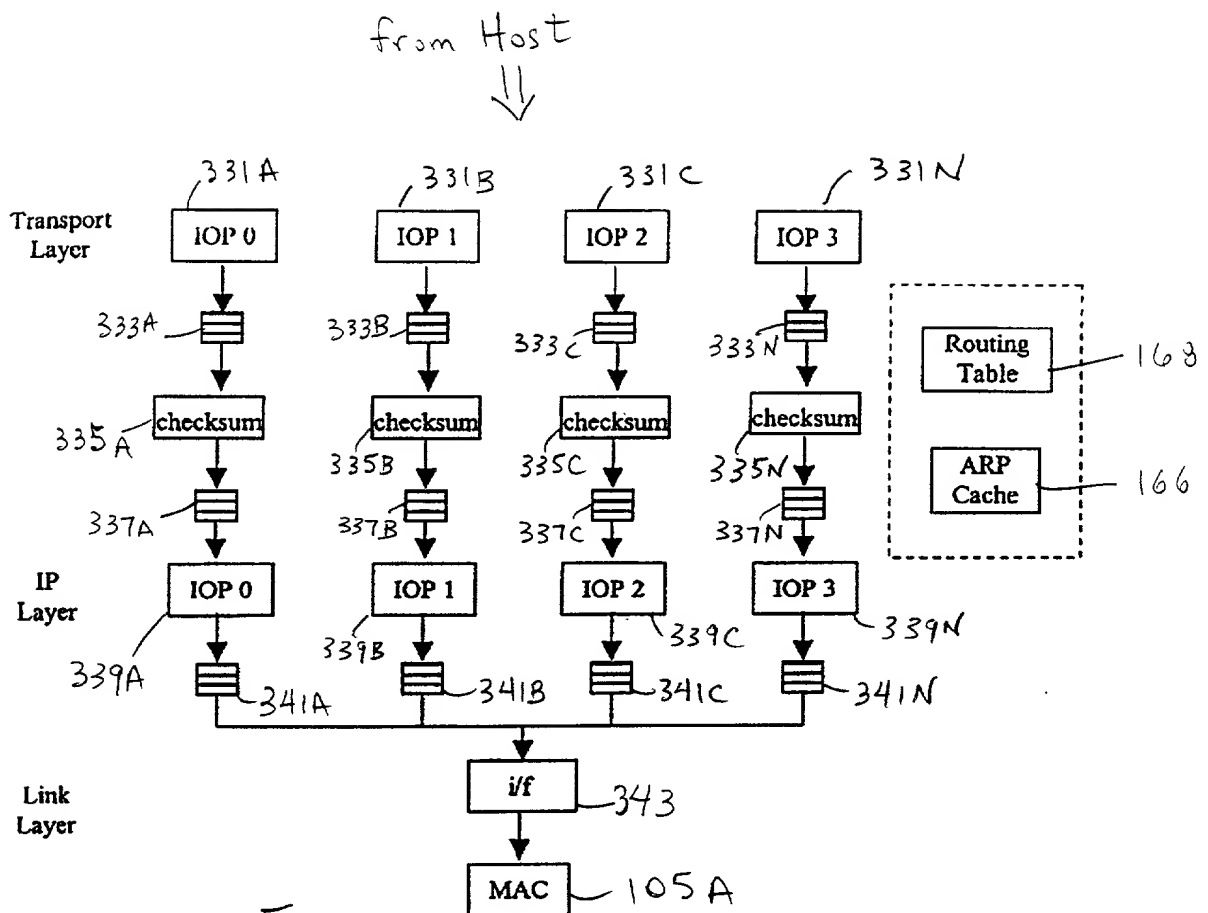


Figure 10A

The packet-sending path.

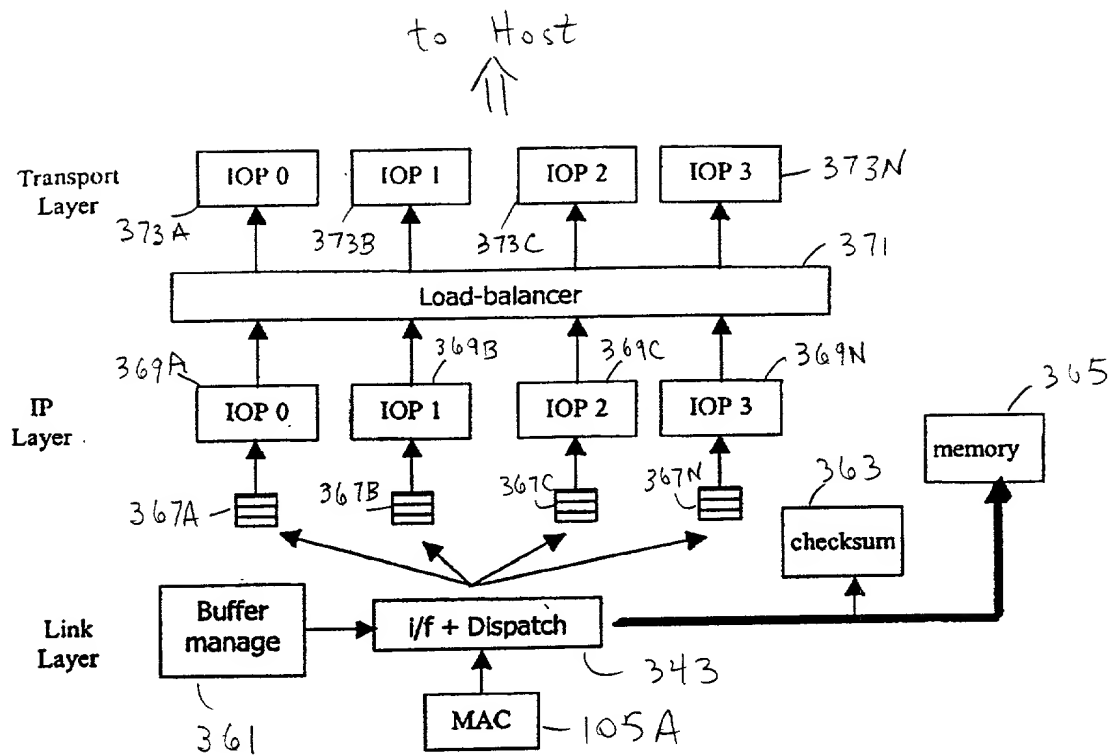


Figure 10B
The packet-receiving path.

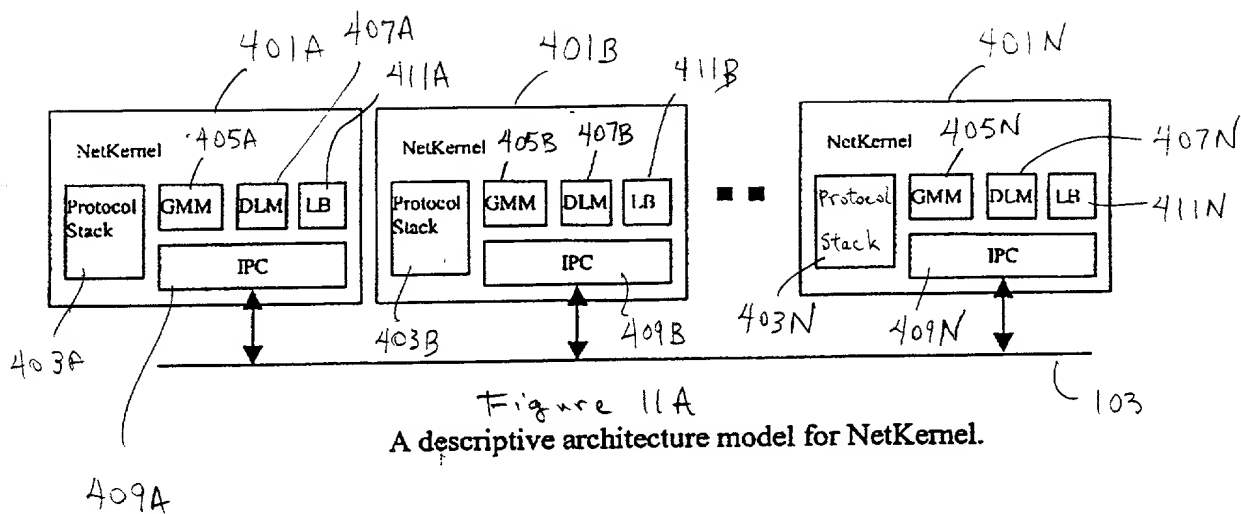
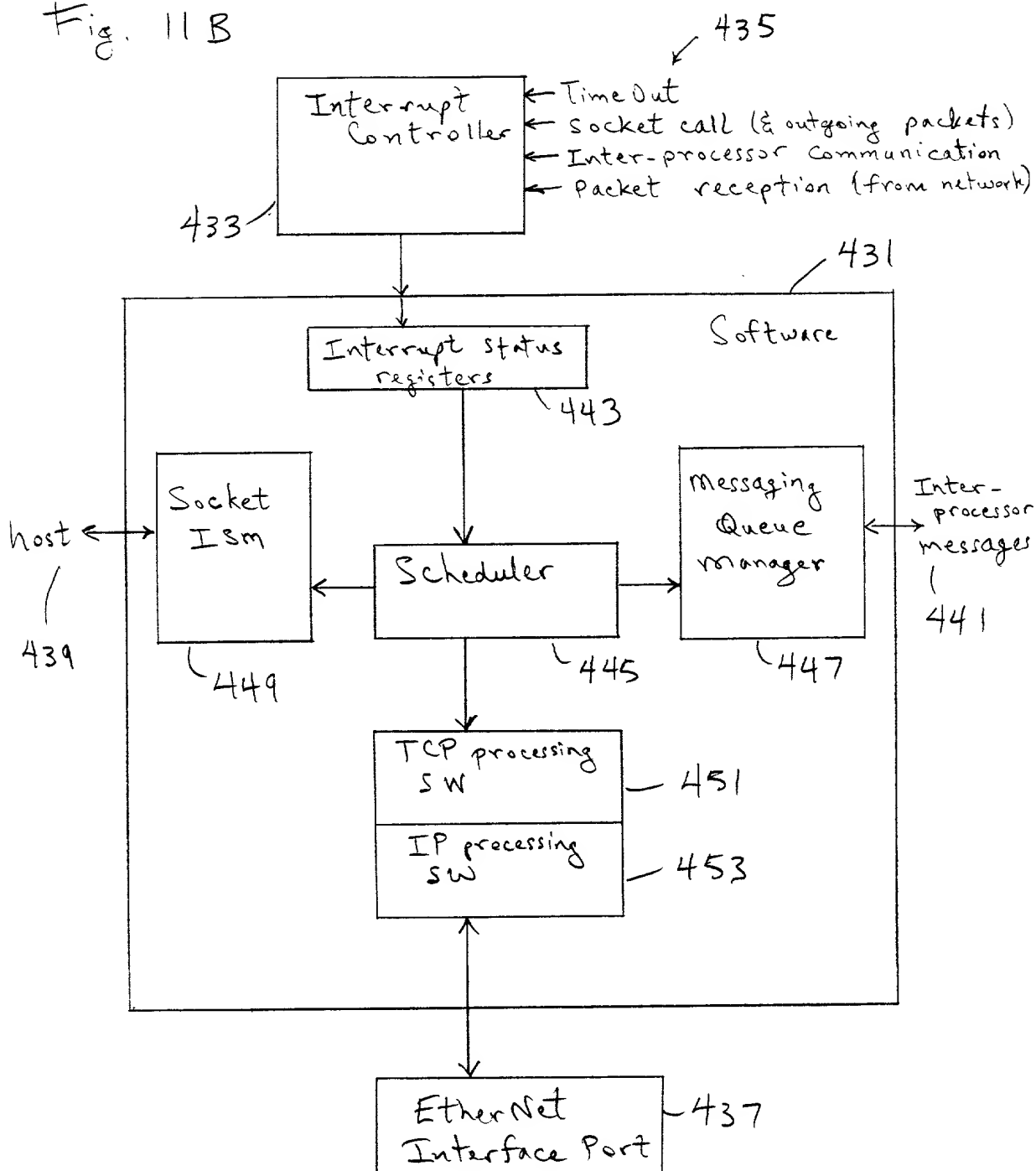


Fig. 11B



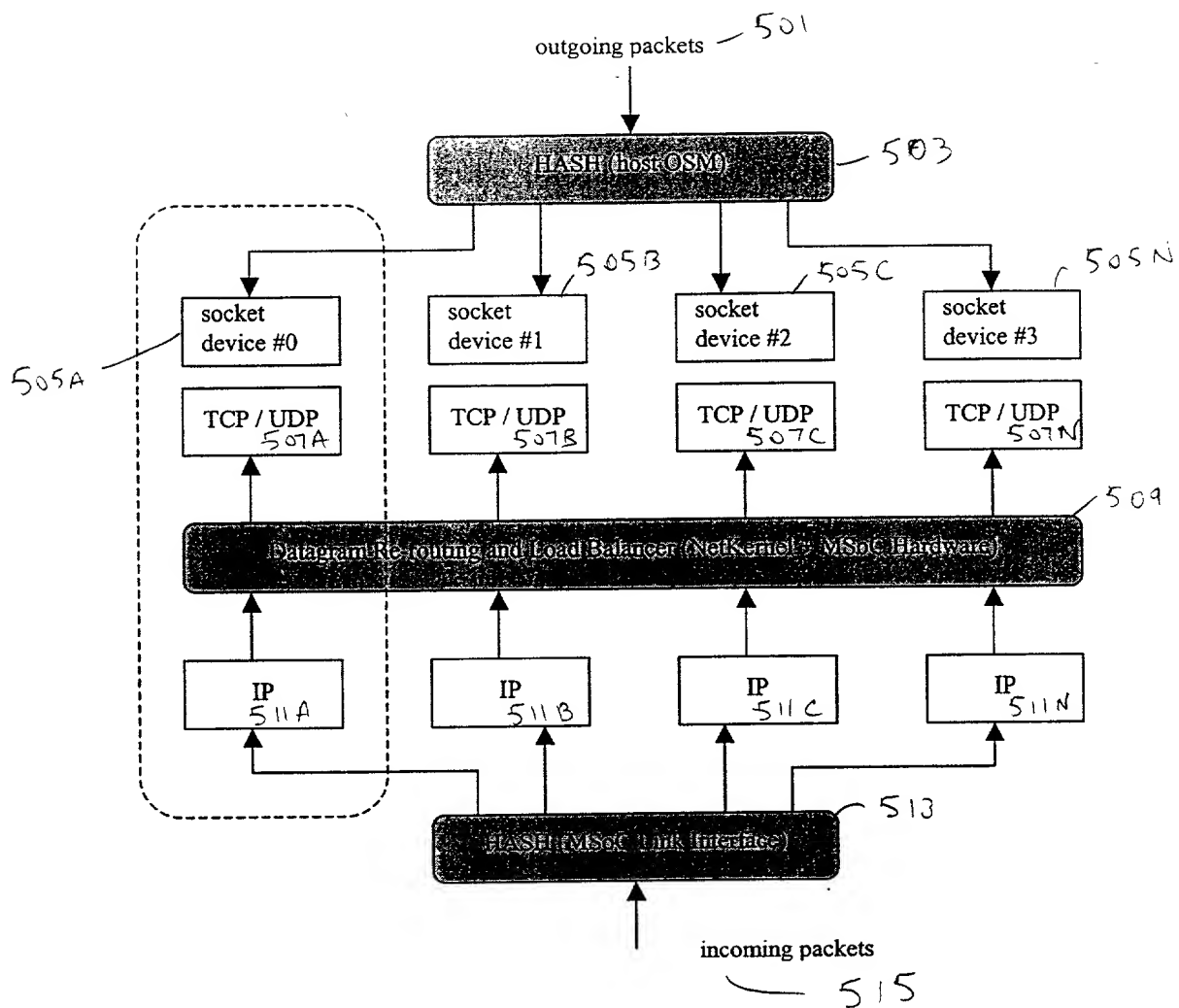


Figure 12A

An illustration of packet flows for load balancing.

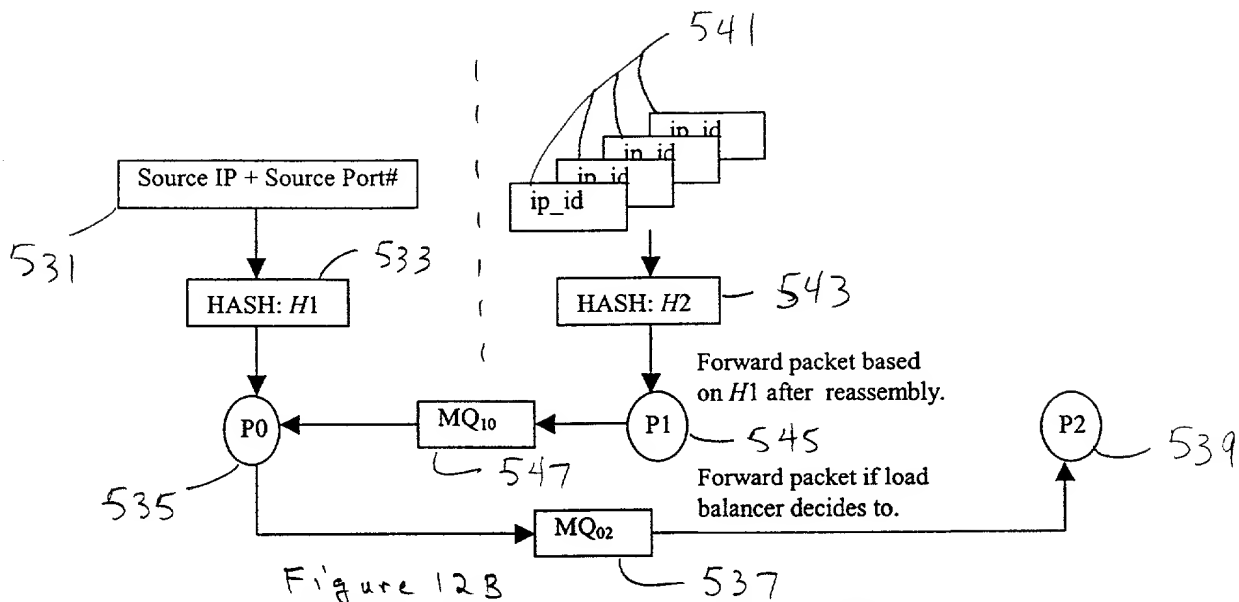


Figure 12B
Illustration of directing packets on address hashing and load balancing.

Figure 13

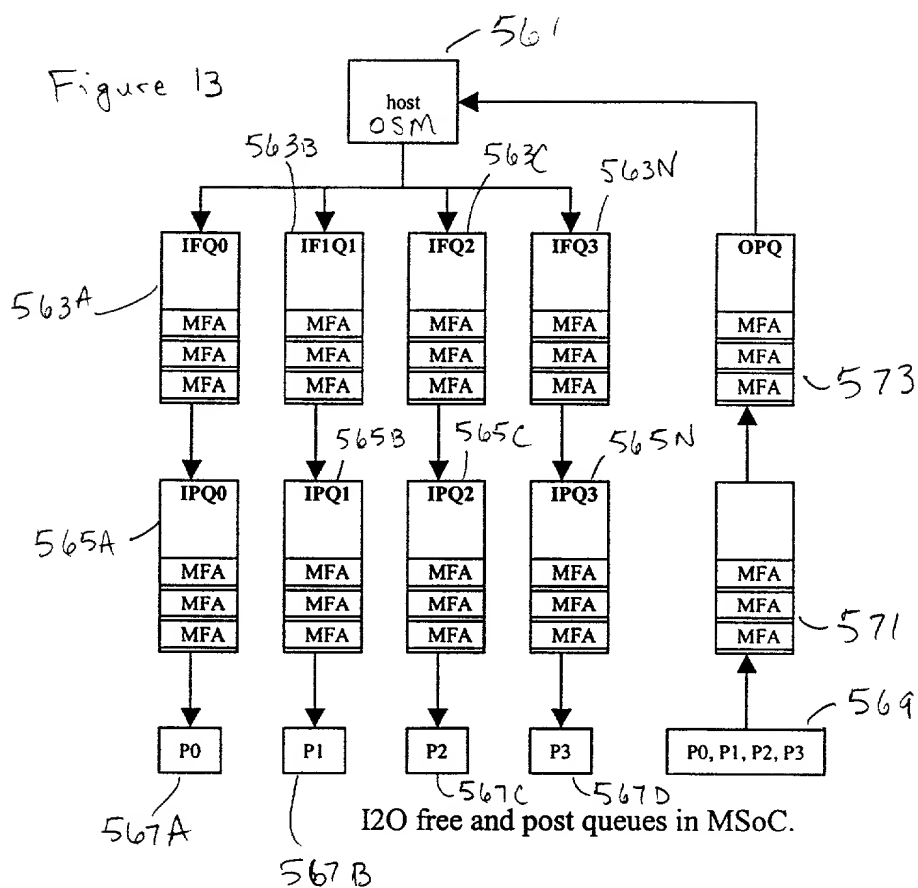


Figure 14

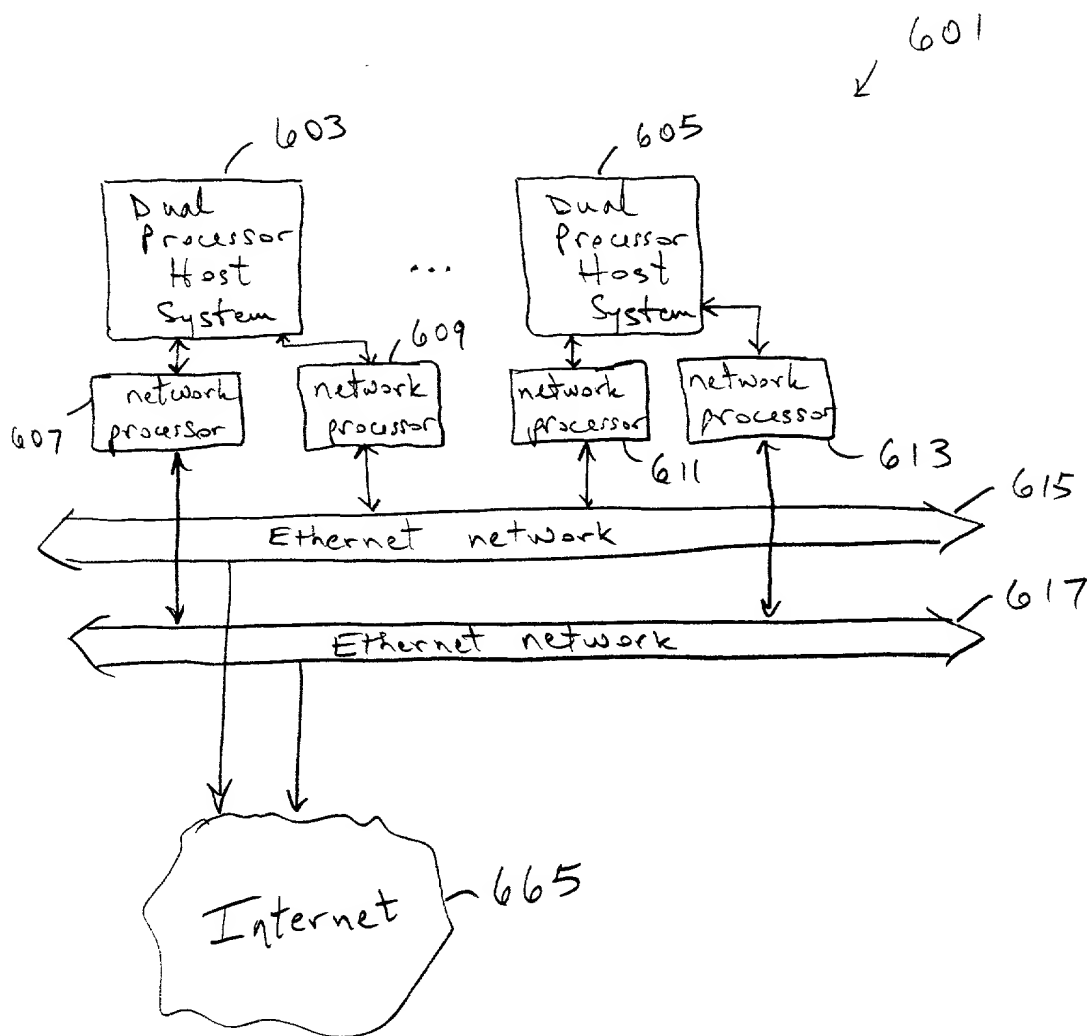
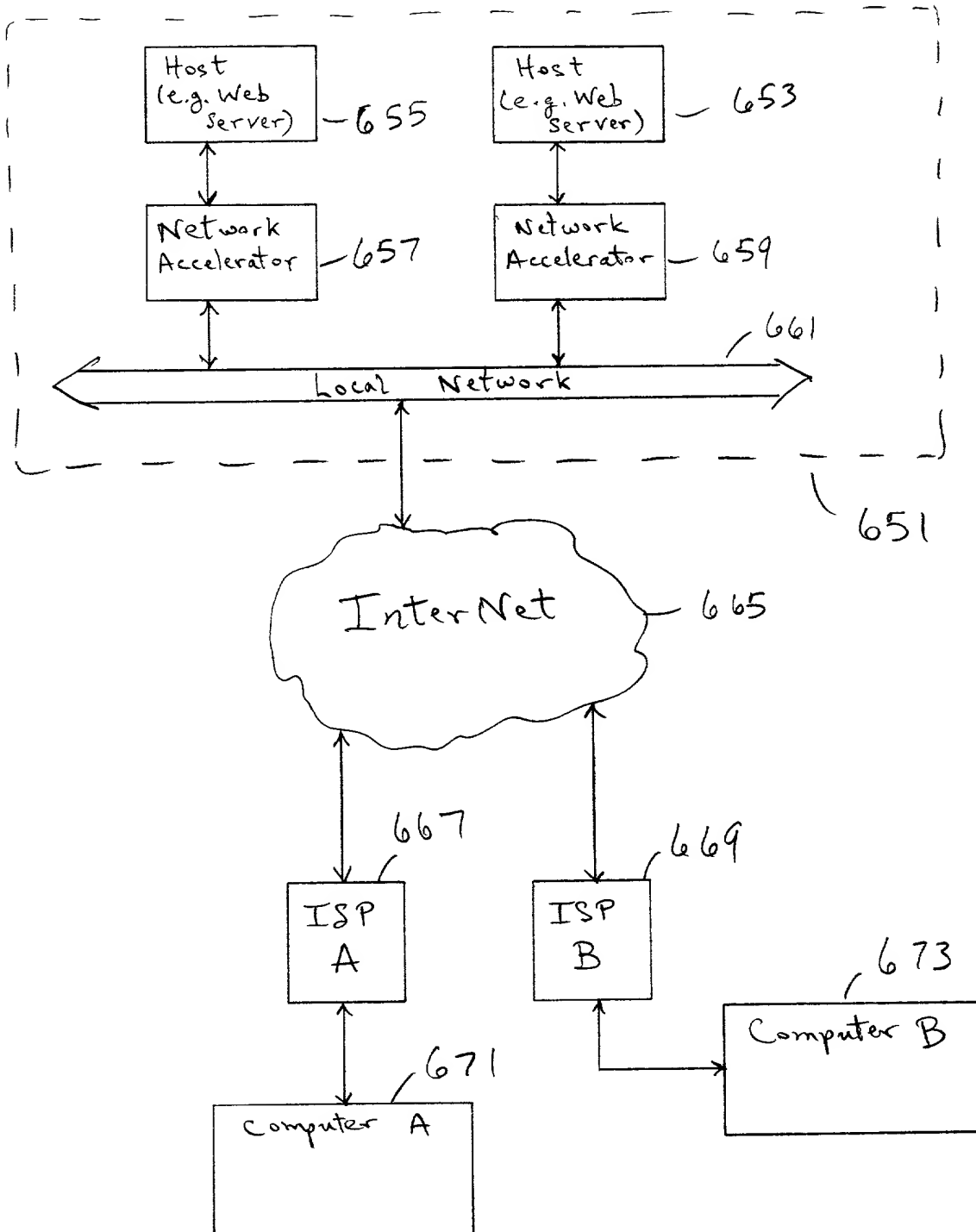


Fig. 15



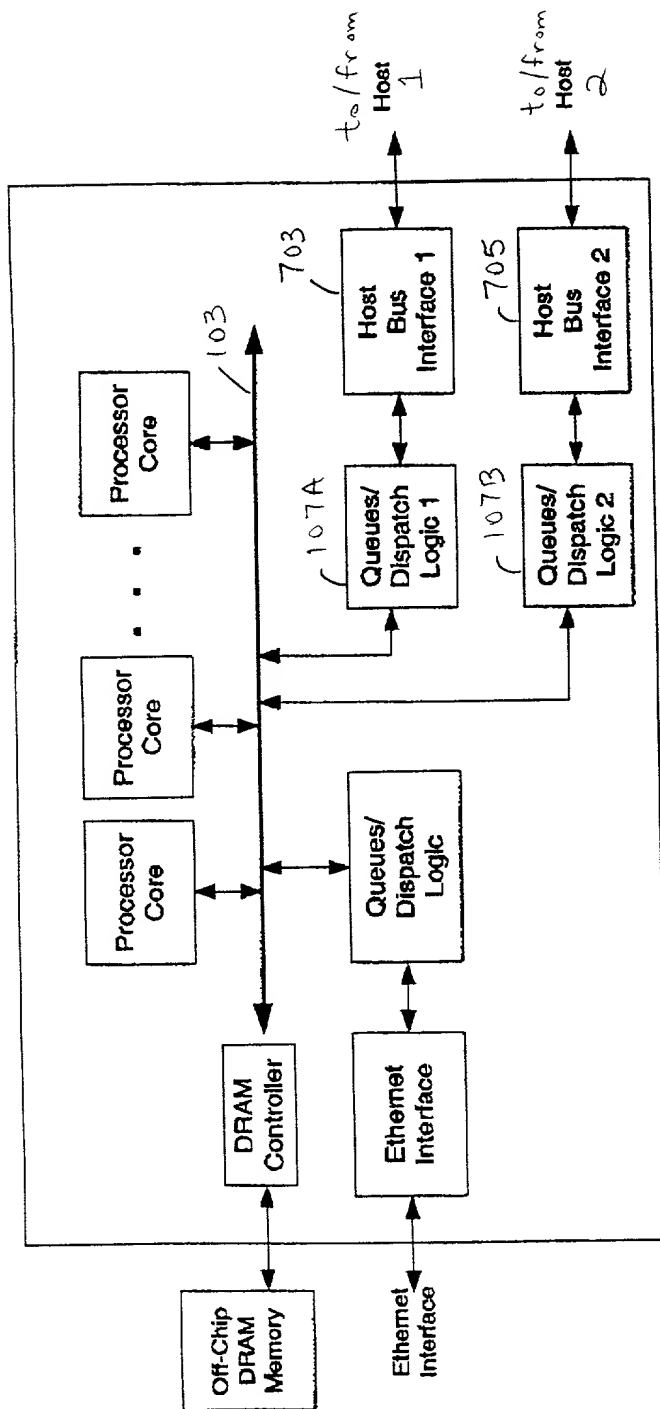
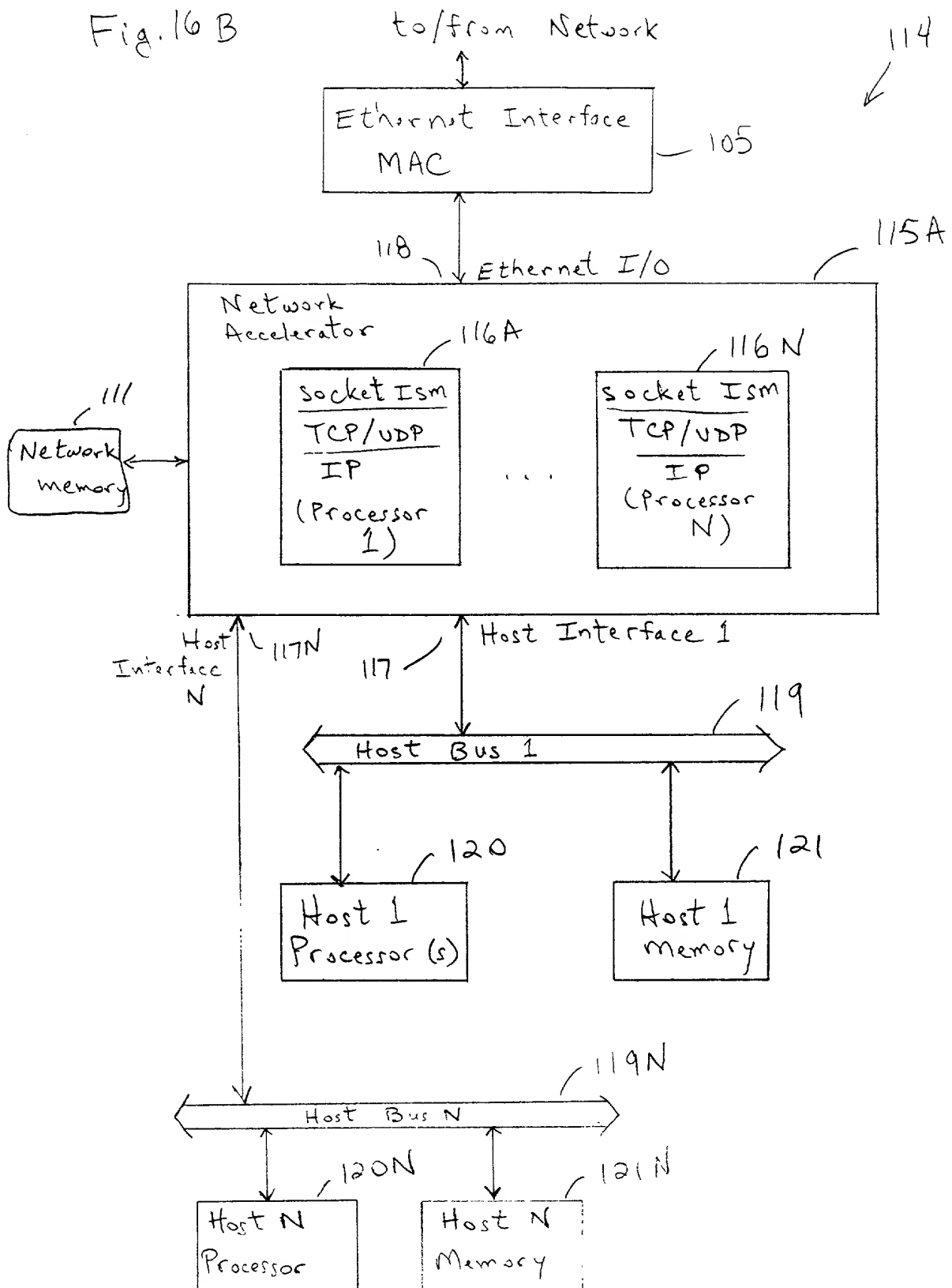


Fig. 16 A

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Fig. 16 B



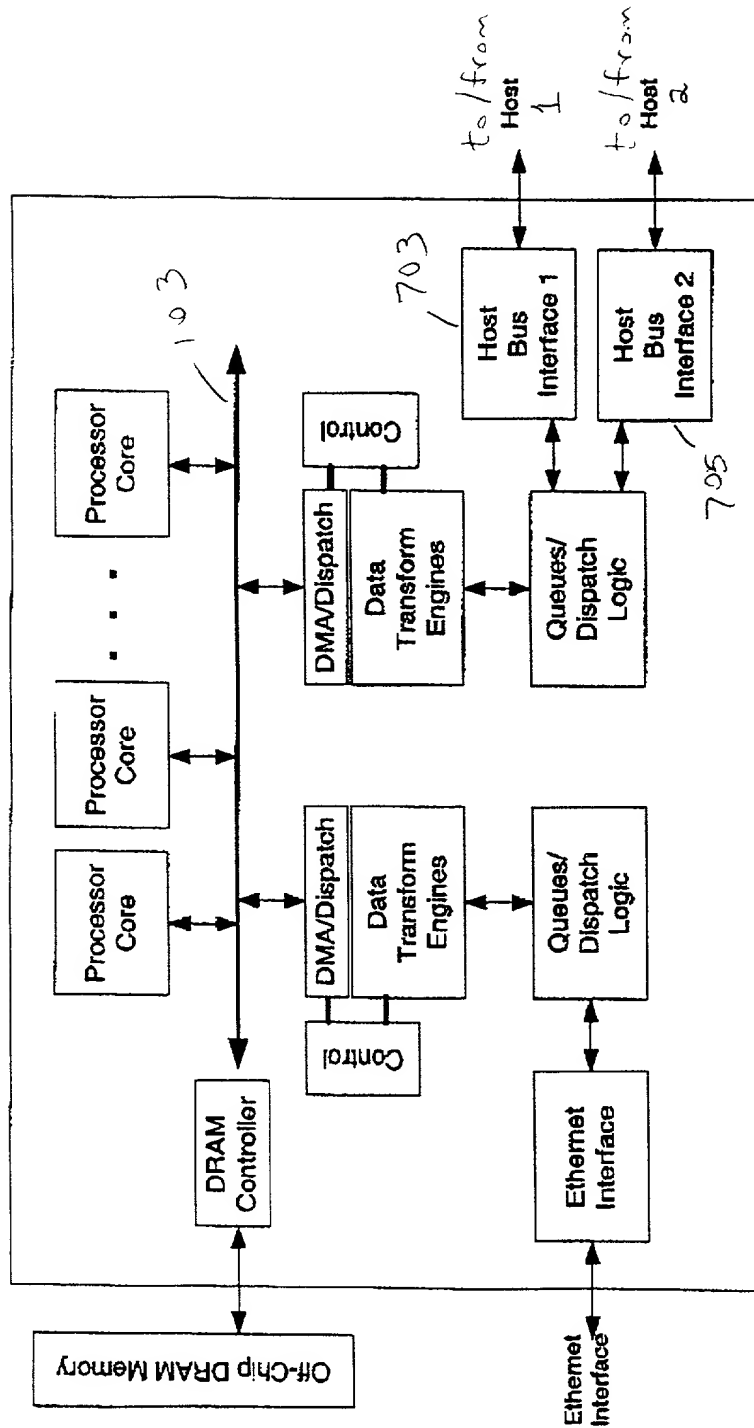
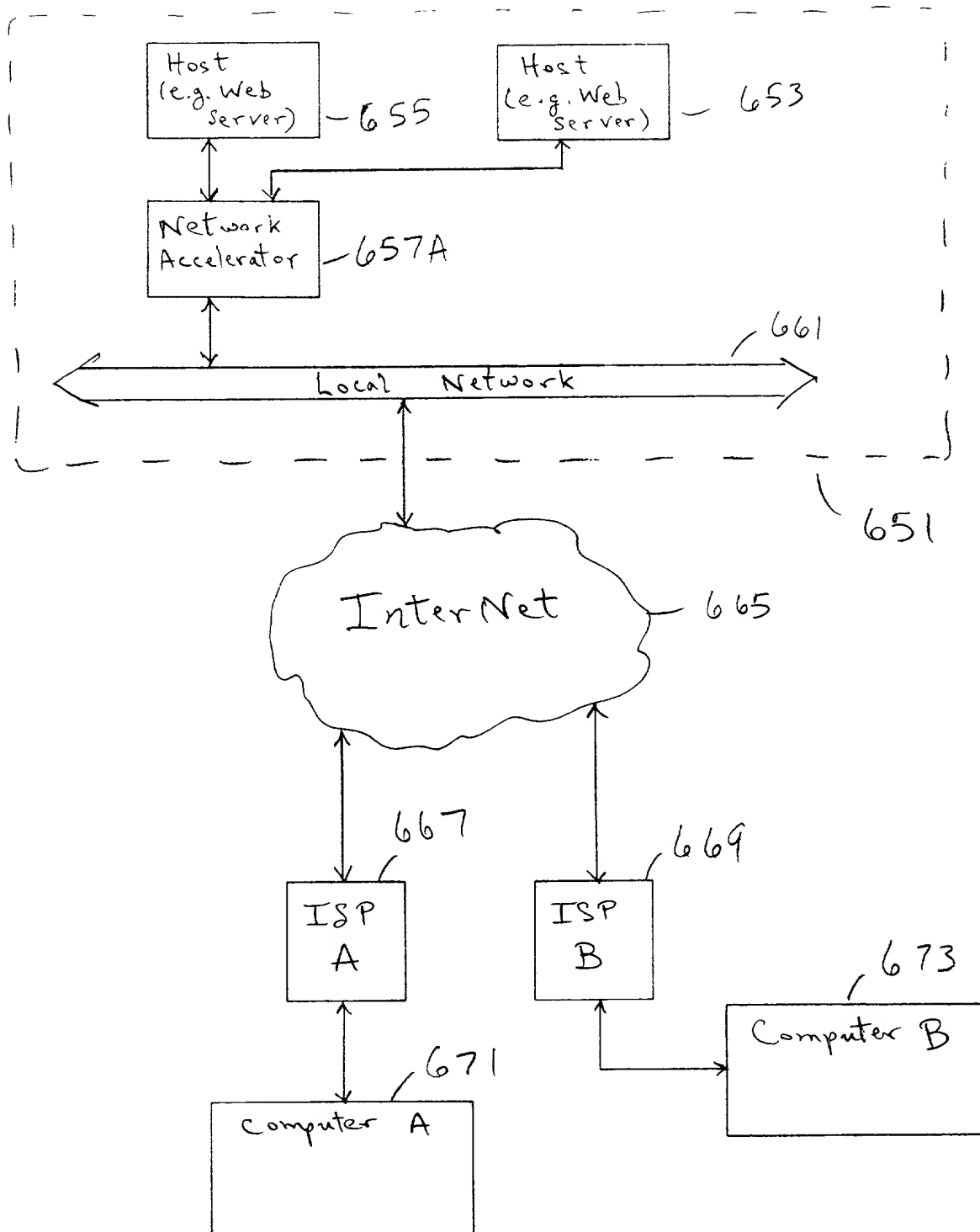


Fig. 16C

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Fig. 16D



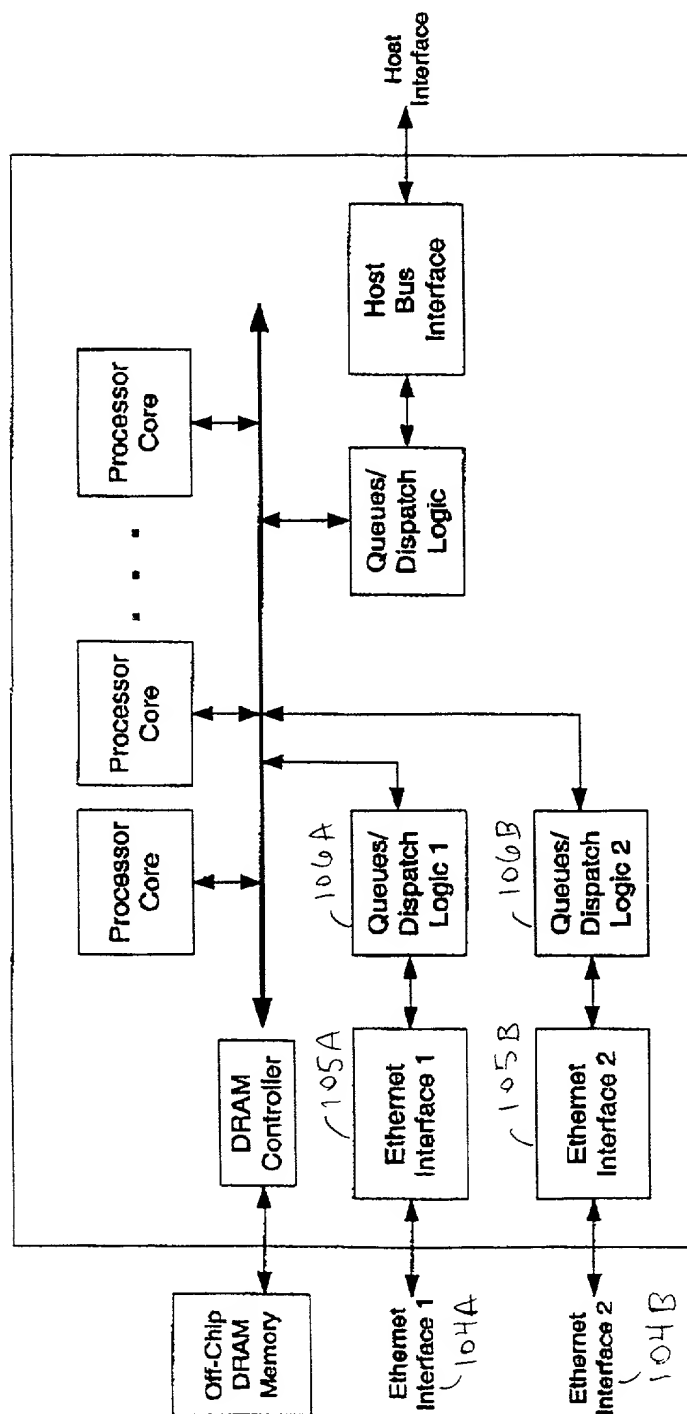


Fig. 17A

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Figure 17 B

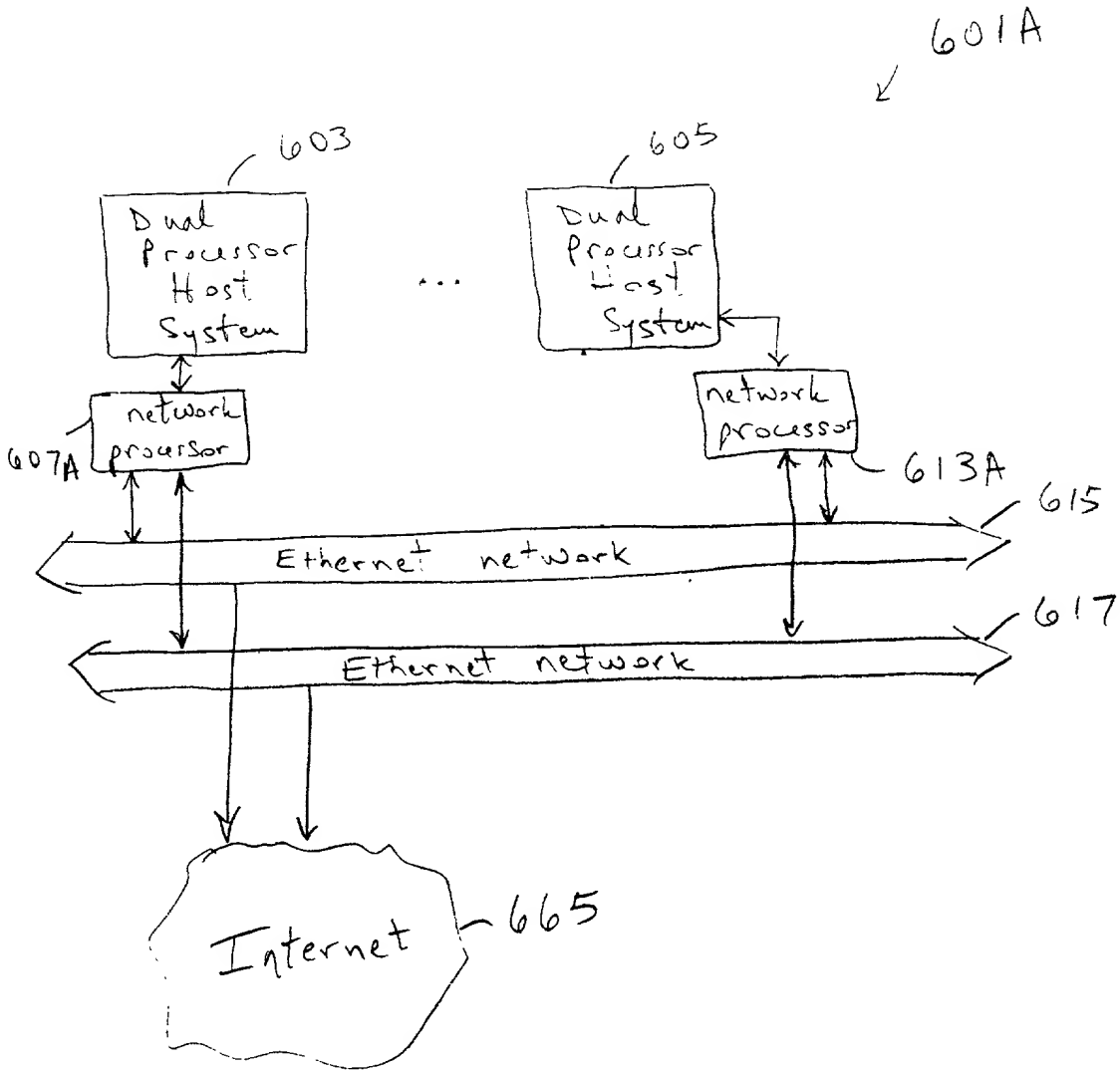


Fig. 17C

